CmpE 59D: Special Topics in CmpE: Design Automation for Embedded Systems

Instructor: Arda Yurdakul

Assistant: Görker Alp Malazgirt (CASLAB)

Motivation:

Today design tools are mature enough for SW engineers to make designs on HW. With the advent of parallel and configurable (in SWE jargon, configurable is equivalent to programmable) hardware, more opportunities exist for non-HW engineers to make designs on FPGAs, which is a fully configurable HW for any application. Hence, due to its full configurability, FPGAs are widely adopted in current embedded systems. FPGAs are also promising solutions for the next generation computing systems. So, in this course, our first aim to teach non-HW engineers how to make HW design from a given C code.

On the other hand, today there are lots of computing options for an embedded systems engineer: single core, multicore, GPU, FPGA, multi processor + FPGA, dataflow… Which one is more suitable for your application? How much cache, how much memory is required? In this course, we will also make non-HW engineers learn tools to select the best solution for their problems.

Tentative Course Outline

Week 1: Introduction:
Why do we need design automation in embedded systems? Embedded Systems properties. Design requirements. Current embedded system platforms. What is next?

Week 2: Components of design automation (DA)
A brief info about DA: design exploration, design tools (properties of tools in system level DA, high level DA, Electronic DA (EDA), simulation)

Week 3: Where do we start: Representation of embedded systems.
Definition of a Model. Models of computation and/or communication: Graphs. Dataflow. Control flow. Petri Nets. Synchronous Data Flow (SDF) Process Networks (PN)
Announcement of HW1 (on paper with pencil :)

Week 4: Design Entry: Application
Modeling languages, languages for HW/SW codesign, high level languages, intermediate representation generation

Week 5: Design Entry: Architectures
Computation: multicore, gpu, fpga, custom/extensible CPUs, dataflow machines, accelerators, soft cores
Communication: high-speed bus, NoC
Memory: Scratchpad, stream, multiport.
Submission of HW1(Week 5).

Week 6-7: Lots of choices exist. How to select: Design Space Exploration
Constructing a design exploration space. Pareto points. Search directions. System Simulation.
Tool: Multicube, Multi2Sim,
Announcement of HW2 (Week 7)

Week 8: Design: Tasks in DA
Given a cost function solve one or some of the following problems under given constraints: Allocation-Binding-Mapping-Partitioning-Placement- Routing-Scheduling.

Week 9-10: Mapping to hardware from C/C++: High Level Synthesis
Design with constraints. Data Representation. Pipelining. Loop unrolling. Loop merging. Logic Simulation.
Tool: Vivado HLS and Simulator.
Submission of HW2 (Week 9). Project announcements (Week 10)

Week 11: HW2 Presentations and Demo

Week 12: Midterm

Week 13: Projects Related Lecture

Final: Final Project Presentations and Demo

Reading Material

Related material (blogs, articles, manuals, book chapters) will be announced at each lecture.

Grading

HW 1: 15%
HW 2: 35%
Midterm: 15%
Final: 35%